LIDINE 2015

Signal Processing and Electronic Noise in LZ

2015/08/29
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On behalf of the LZ collaboration
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Topics

- Electronics in LZ
  - Focus on Xe space PMTs
- Signal processing
  - Noise
  - Gain linearity
- Electronic chain test
  - Setup
  - Goals

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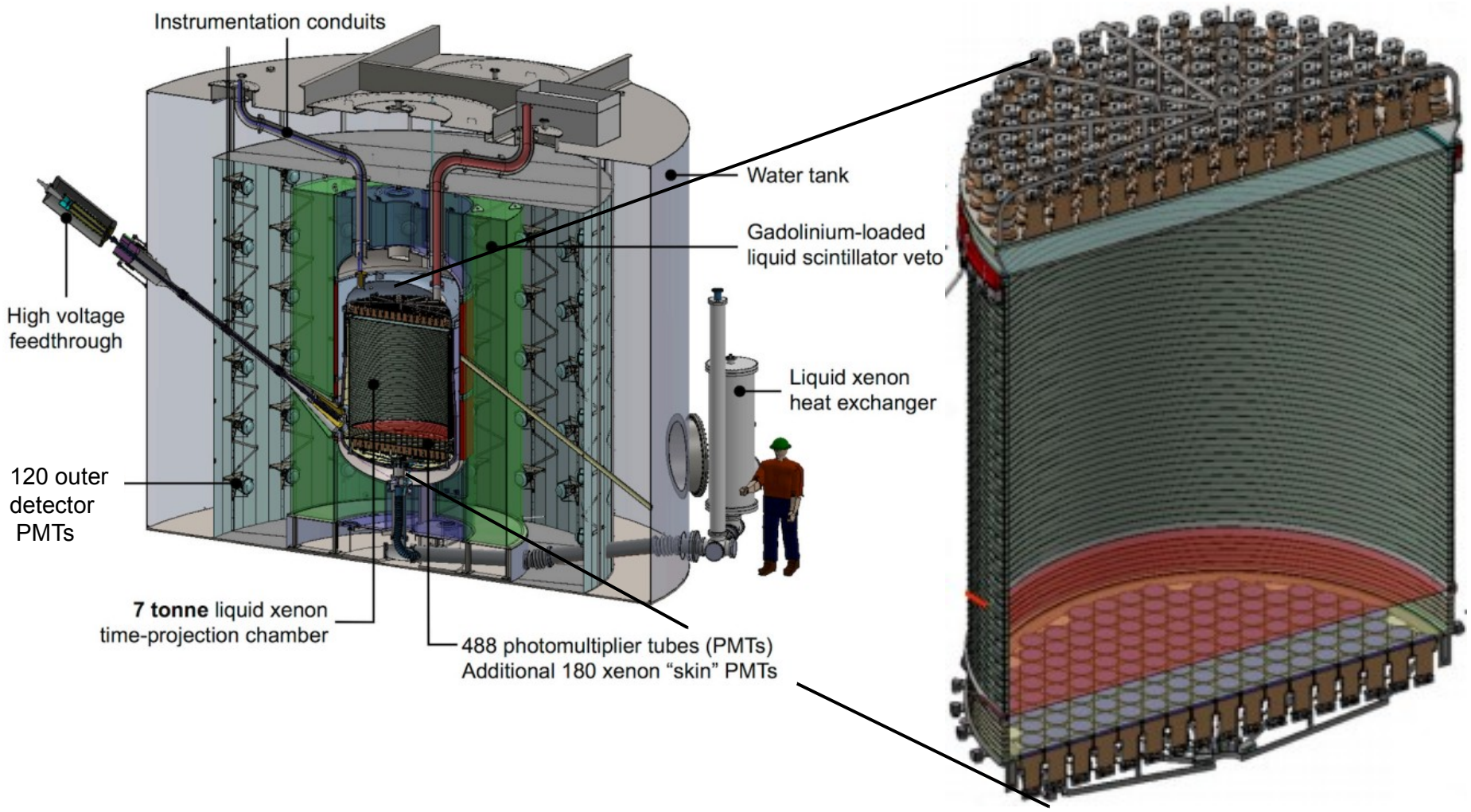
LZ Detector Overview



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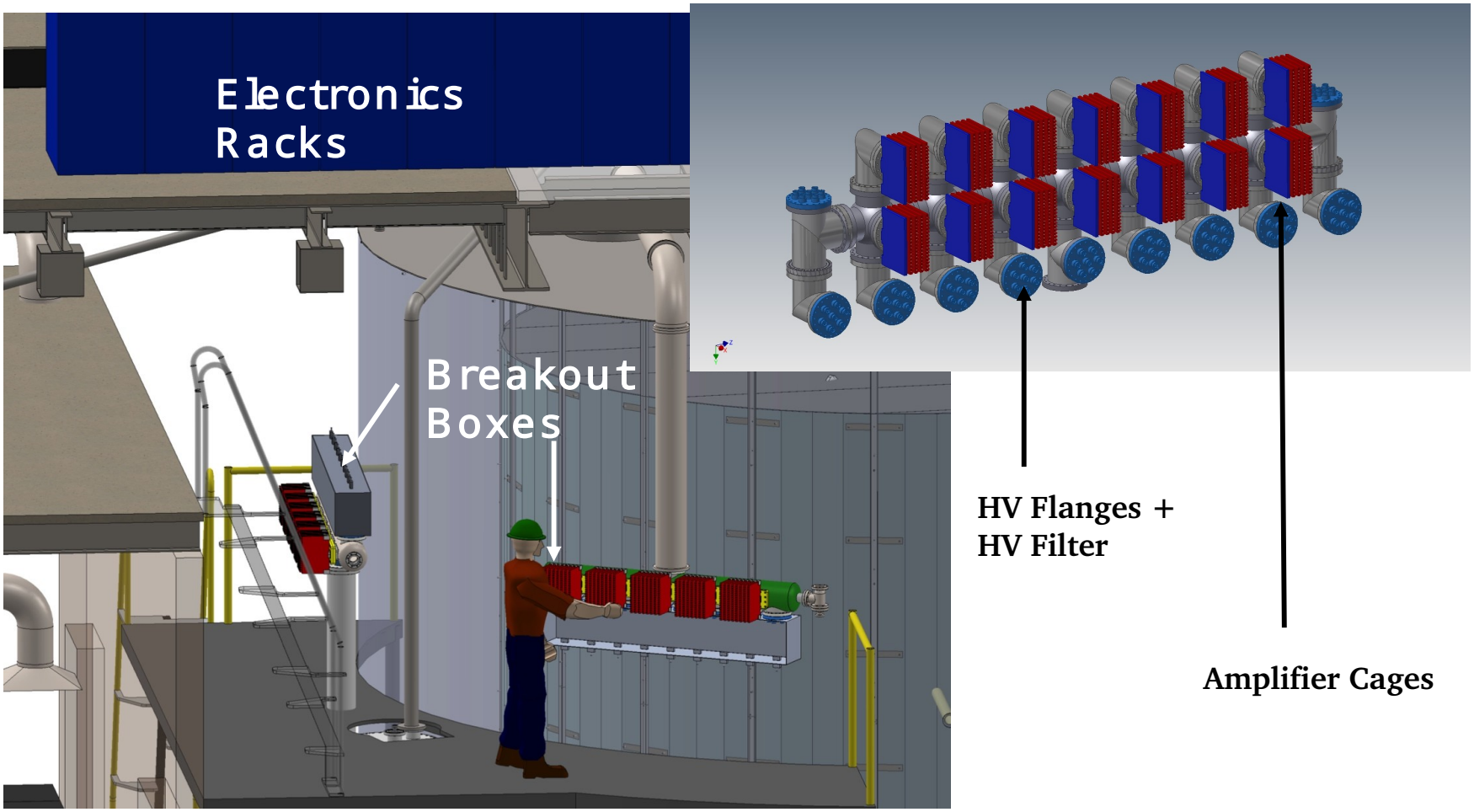
Electronics in LZ - I



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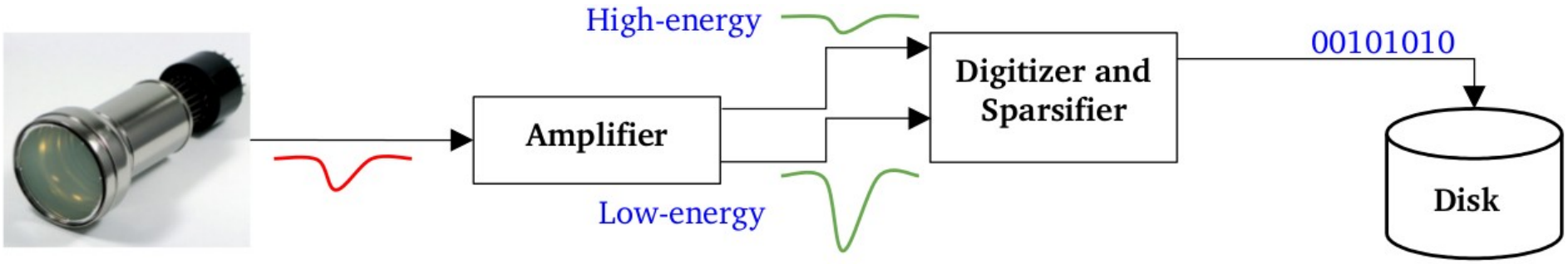
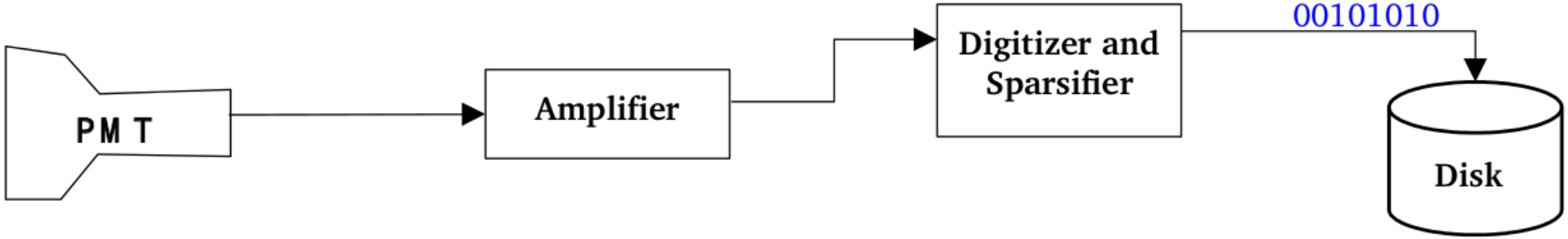
Electronics in LZ - II

- 488x R11410 PMTs for Xe TPC



- 180x R8520 PMTs for the Xe skin
- 120x R5912 PMTs for the outer detector



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Electronics in LZ - Cables

Cable Type	Type	Length (ft)	Additional Specifications
Internal Cables			
Signal/HV from Xe PMTs	Gore 3007	45	low heat load, low background, low signal attenuation
External Cables (low smoke zero halogen)			
High Voltage	Kerpen-48 core	56	
Signal	LMR-100A-FR	56	low signal area attenuation
Logic	LMR-100A-FR	2	
Network	Belden 7936A	Varying	
HDMI	TBD	TBD	low signal loss

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Signal Processing - Pre-prototype Amplifier

- Pre-prototype tested in Spring ‘14
- Xe TPC PMTs amplifiers design specifications:
  - Dual gain output
  - 4 output channels/ input channel
  - High-energy (HE) channel
    - Shaping time (FWTM) of 30 ns
    - Area gain of 0.5
  - Low-energy (LE) channel
    - Shaping time (FWTM) of 60 ns
    - Area gain of 20
- Design requirement: total front end electronics noise <0.5mV

Pre-prototype
designed at UC-Davis

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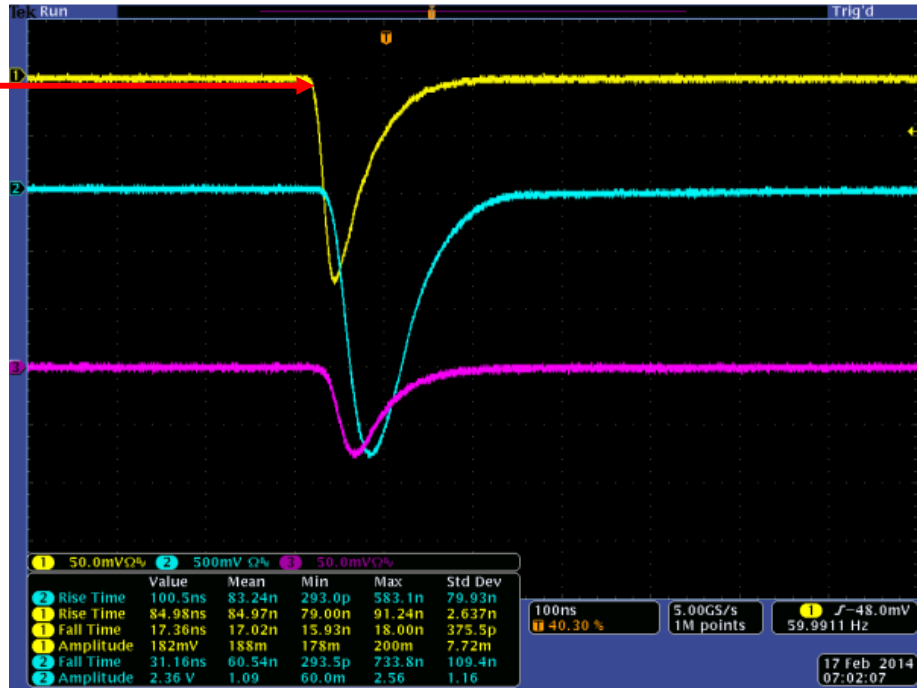
Signal Processing - Test Results

- Performance evaluated with fast and slow pulses:
  - Fast pulses:
    - 10 - 50ns risetime
  - Slow pulses:
    - Gaussian pulses
    - 150 - 1500 ns risetime

- Test Results:
  - Area gain matched specifications
  - Noise within acceptable bounds
  - Could not measure crosstalk (crosstalk < 0.5%)
  - HE shaping is fine. LE shaping needs changes



(Yellow) Input pulse to pre-prototype amplifier: 180mV, 17ns
(Cyan) Low-energy channel
(Pink) High-energy channel

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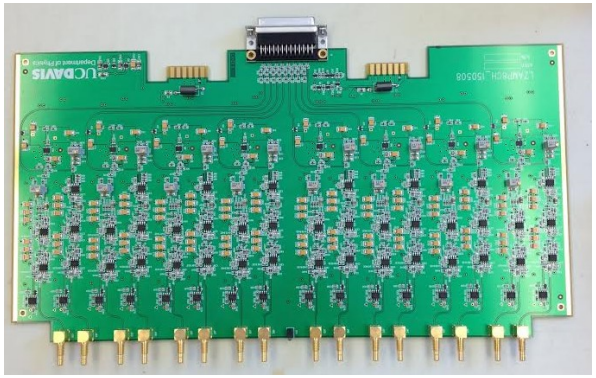
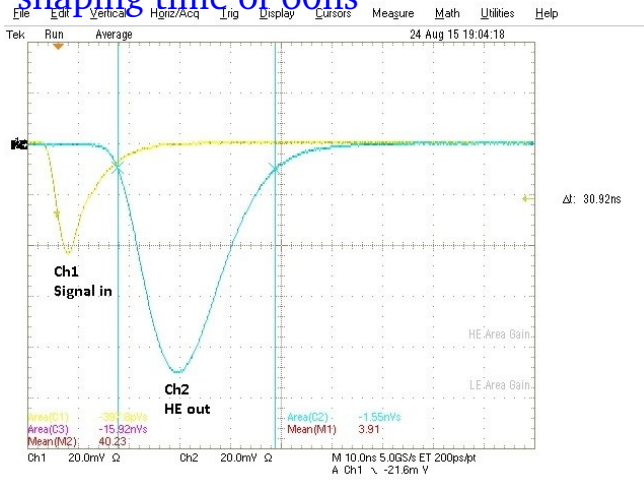
Signal Processing - Prototype Amplifier

- New Xe TPC PMTs amplifiers design specifications:
  - 2 outputs/input channel
  - 8 input channels/board
  - High-energy (HE) channel
    - Shaping time (FWTM) of 30 ns
    - Area gain of 4
  - Low-energy (LE) channel
    - Shaping time (FWTM) of 60 ns
    - Area gain of 40
- Shaping time now matches specifications
- New design to be tested in Fall ‘15



(Left) Prototype designed at UC-Davis

Low-energy channel output with shaping time of 60ns



High-energy channel output with shaping time of 30ns

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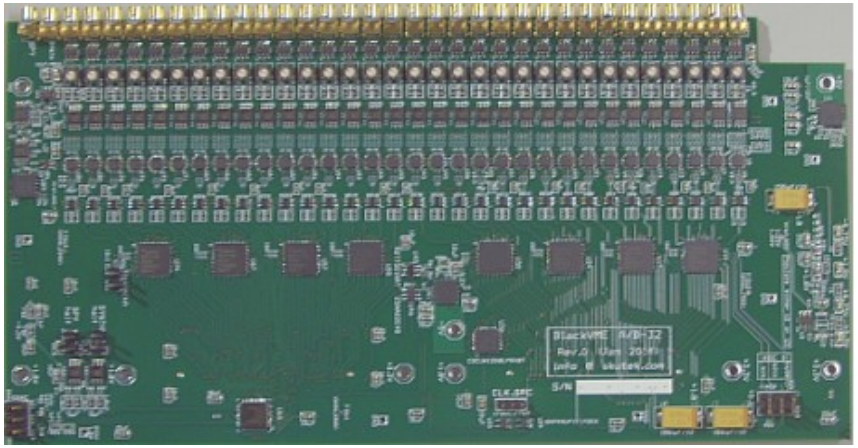
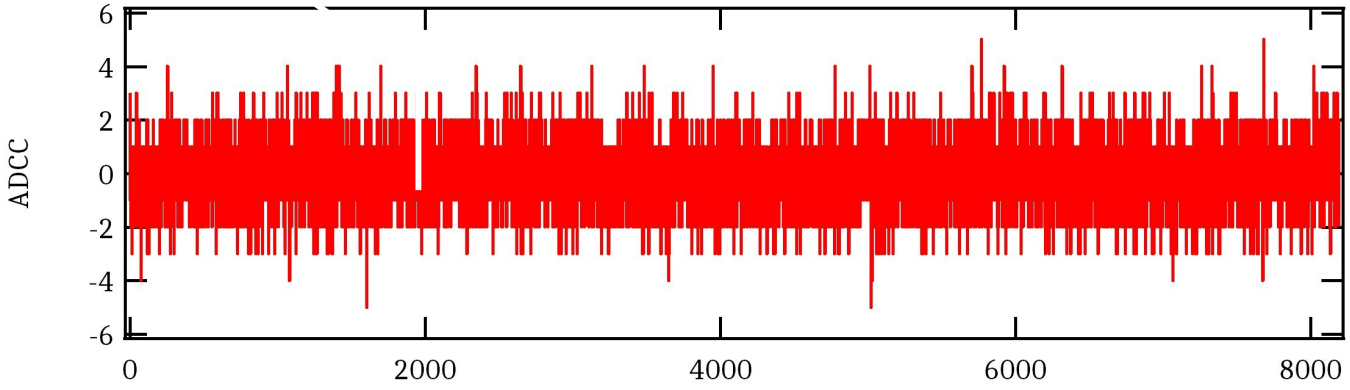
Signal Processing - Digitizer

- Digitizer design specifications:
  - 32 input channels/board
  - 100 MHz sampling frequency
  - 14 bit resolution
  - 2 V dynamic range
- Total front end electronic noise (RMS):
  - DDC32: 1.19 ± 0.02 ADCC
  - HE + DDC32: 1.22 ± 0.02 ADCC
  - LE + DDC32: 1.58 ± 0.02 ADCC
  - <0.5mV (4 ADCC) noise per channel



DDC32 daughter card designed by SkuTek.com



Noise Waveform

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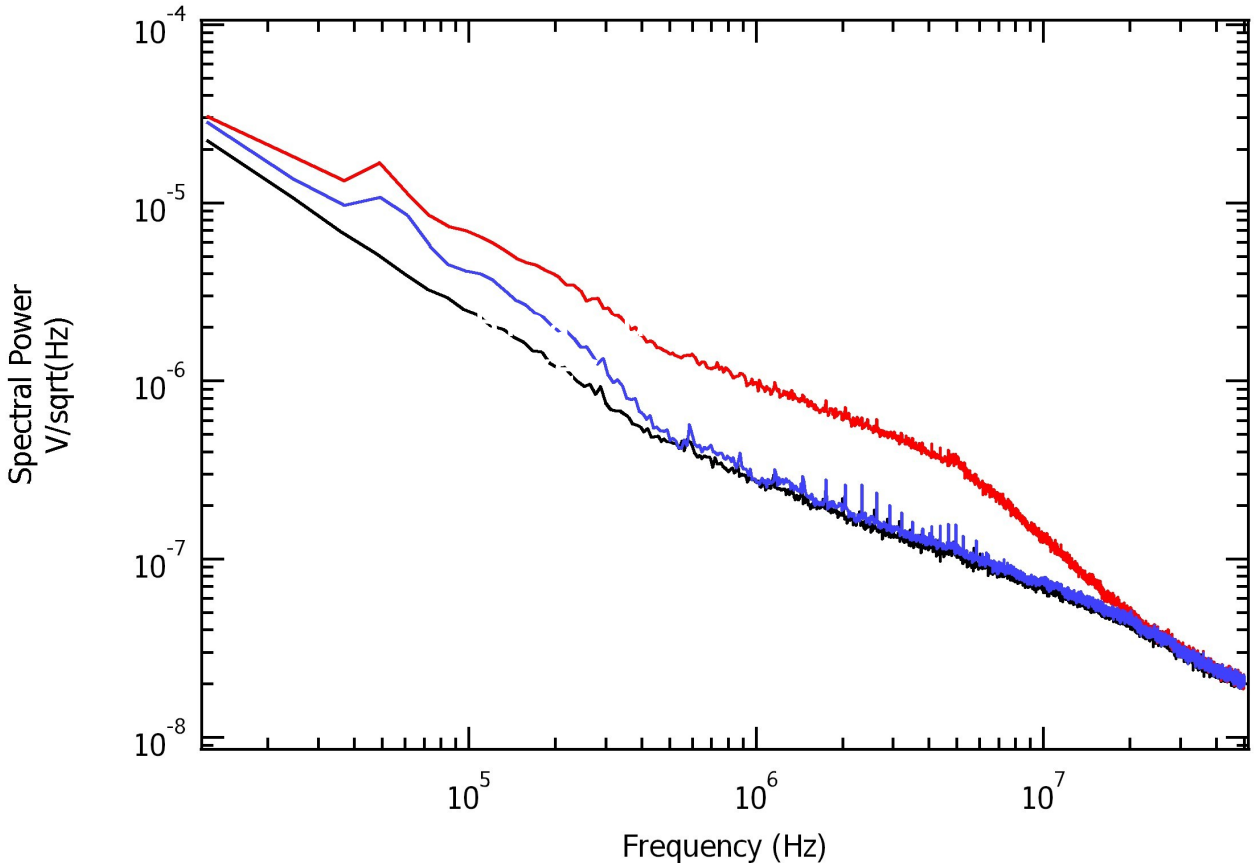
Signal Processing – Noise Measurement

- Averaged Fourier transforms of noise waveforms
- Noise falls as 1/sqrt(Hz)
- No predominant noise components



(Black) DDC32
(Red) DDC32 + LE channel
(Blue) DDC32 + HE channel

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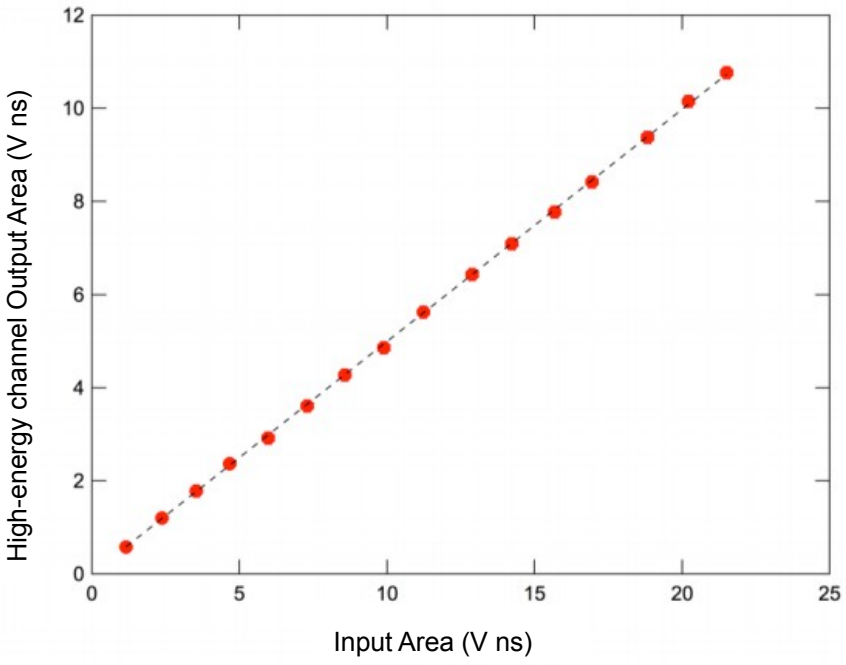
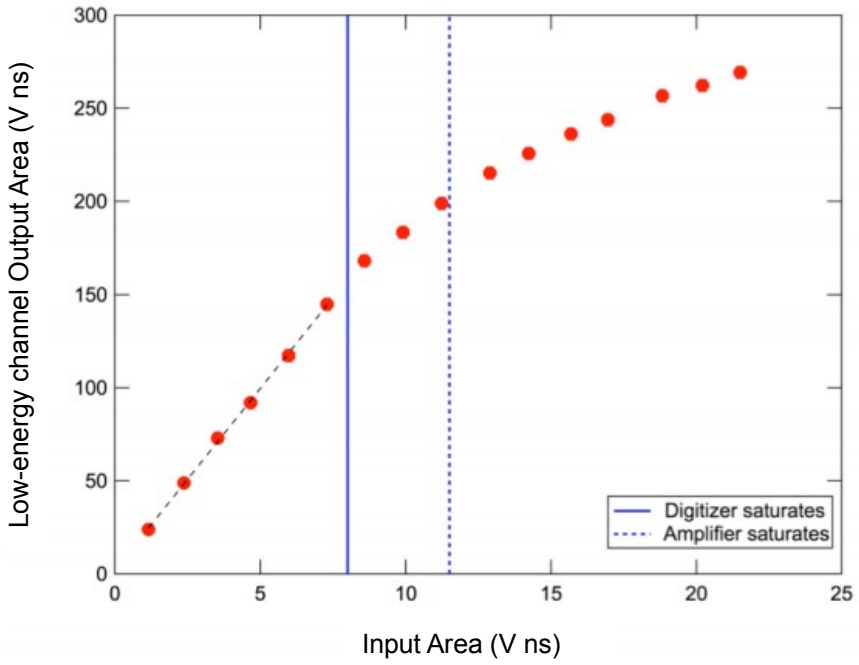
Signal Processing - Gain Linearity

- Measured high-energy channel area gain of 0.5
- Measure low-energy channel area gain of 20
- The digitizer saturates at 1.8V and the amplifier saturates at 2.6V
- Developing methods to recover from saturation
- Below are plots of gain linearity for 20ns fast pulses; errors <1%





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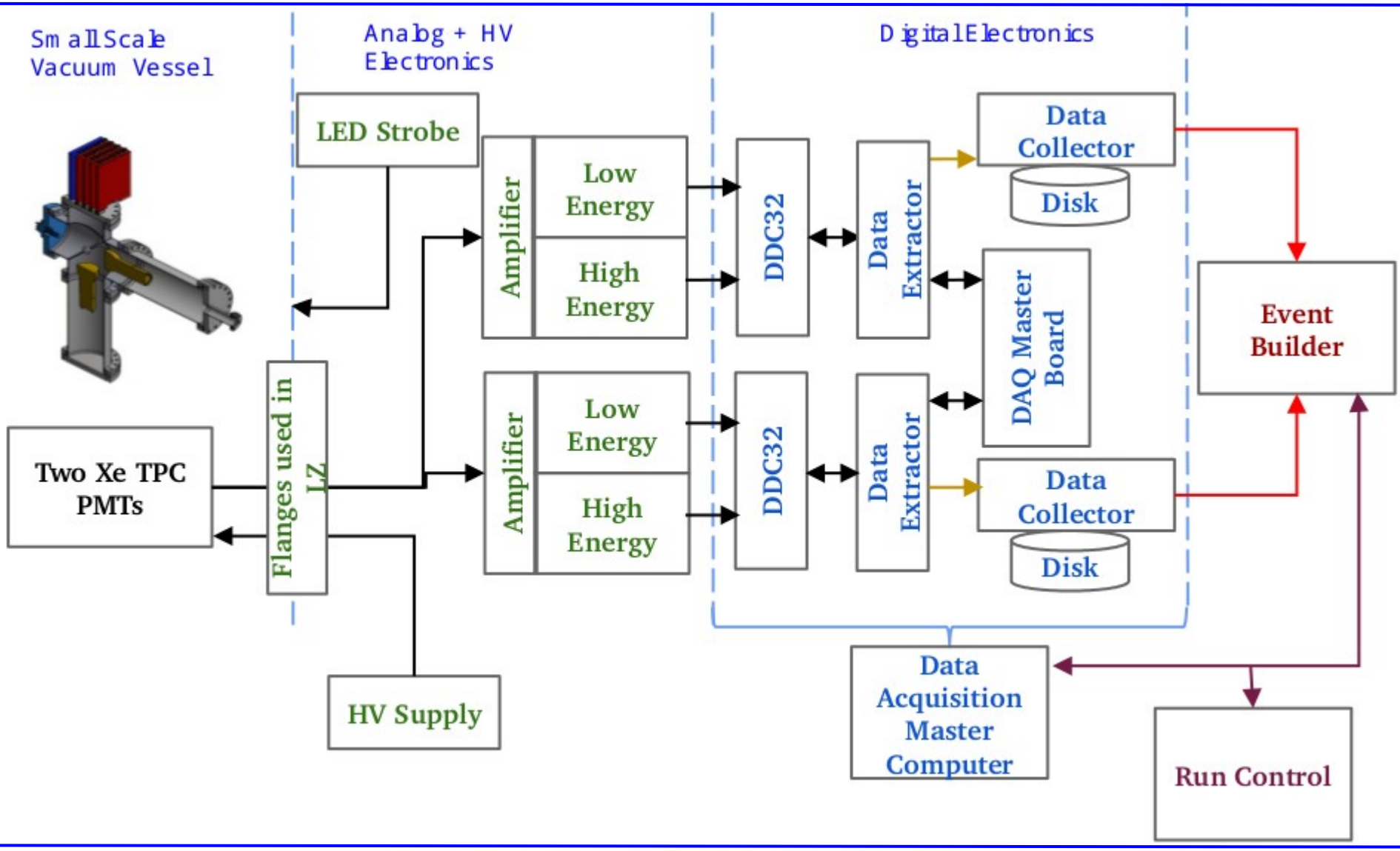
Electronic Chain Test - Setup



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Electronics Chain Test - Setup

- Build a test setup to include:
  - The full LZ electronics chain from PMT to disk on the event builder
  - LZ Xe TPC PMTs and base
  - Signal and HV flanges
  - Connectors and cables with lengths to be used in LZ
  - Hardware, software and firmware that will be used in LZ

- The purpose of the setup is to provide a development system to:
  - Extensively test hardware, software and firmware before deployment in LZ
  - Test every component in the chain
  - Obtain real measurements of performance

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Electronics Chain Test - Goals

- We will stress test this chain and their individual components

- Having two full digitizer and sparsification chains allows us to:
  - Demonstrate how different sparsifiers can work in different modes
  - Evaluate the DAQ master computer and Run Control's ability to monitor and control the setup
  - To see how the event builder handles building events from multiple disks

- With LEDs we will:
  - Generate small and large pulses to study the effect of saturation in the all the components of the chain
  - Generate high pulse rates to stress test the acquisition system
  - Develop techniques to perform PMT timing calibration

- Study what happens when the PMT base saturates

- Study the noise of the full electronics chain

- Develop techniques to eliminate common mode noise

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Thank you

2015/08/29

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Electronics - Cable Attenuation

Cable Type	Length (ft)	Tested Pulse	Area Attenuation (%)	Amplitude Attenuation (%)
Gore 3007	45	2-ns risetime	-18	-56
	90	“	-28	-80
LMR-100A-FR	28	“	-1	-15

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Signal Processing - Test Results

- PDDC 32 saturates at ~2V
- Pre-Prototype Amplifier saturates at 2.6V
- Studying methods to reconstruct pulse area upto 2x saturation voltage within an error of <10%

(Yellow) Input pulse to pre-prototype amplifier: 400mV, 17ns
(Cyan) Low-energy channel
(Pink) High-energy channel

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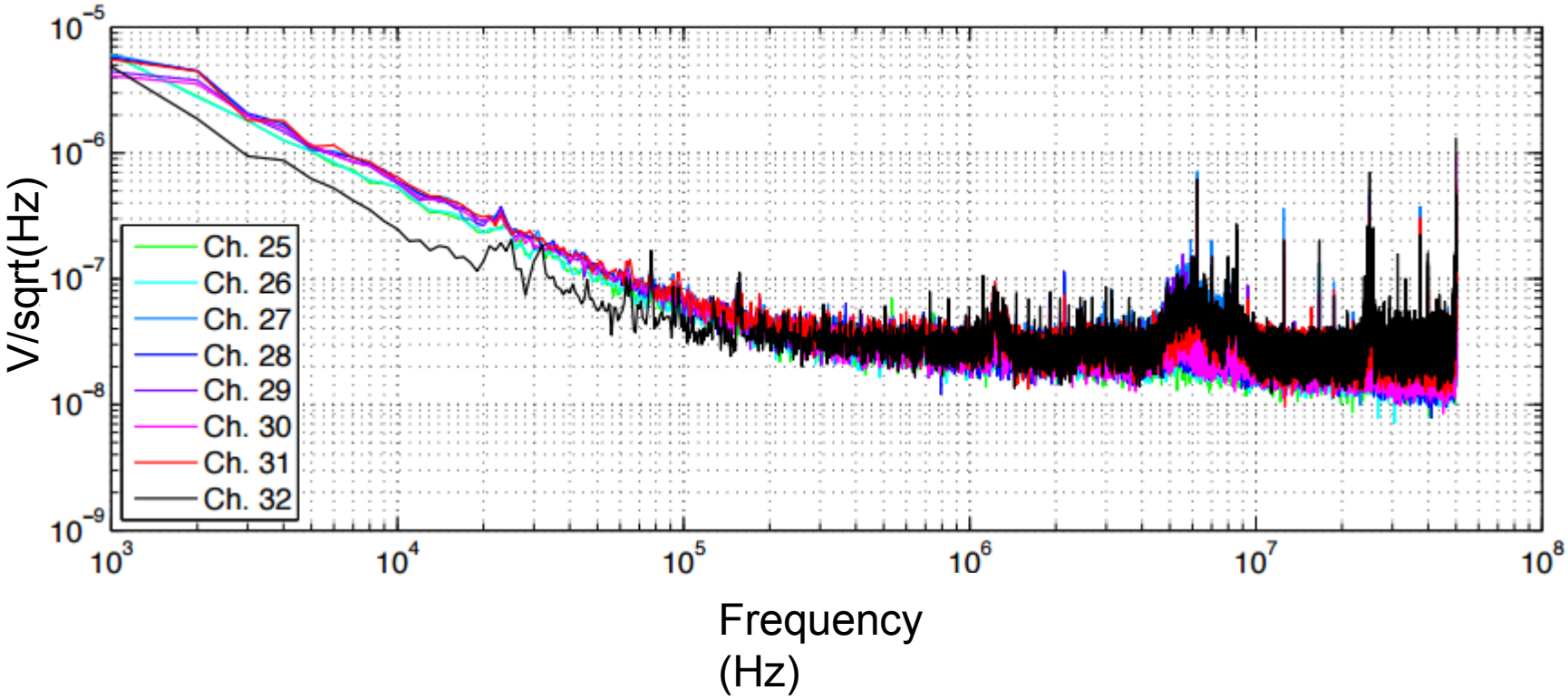
Signal Processing - Noise in LUX



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Electronics Chain Test - Timeline

- Summer ‘15 - Develop Run Control, Event Building, Data Acquisition software and DDC32 Acquisition/Sparsification firmware.

- Sept ‘15 - Deploy code at the machines at the University of Rochester
- Sept ‘15 - Assemble test setup and simulate data with an arb. wavefrom generator

- Oct ‘15 - Test Run Control, Event Building and Data Acquisition software

- Nov ‘15 - Test gain and shaping for various types of simulated pulses
- Nov ‘15 - Receive two R11410 PMTs to integrate into setup
- Nov ‘15 - Integrate the LED strobe into the setup
- Nov ‘15 - Perform PMT saturation study

- Winter ‘15-‘16 - Complete first phase of the electronics chain test

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